AMS and RF Design for Reliability Methodology

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Why is the circuit reliability important?

- Bathtub curve in nanotechnologies
When is the circuit reliability important?

- **Safety critical applications**
  - Biomedical
  - Transport
  - Spatial
  - Energy
  - Security
  - …

- **But today also for**
  - Computer
  - Communications
  - Consumer
Definitions

- **Yield**: the percentage of ‘good’ products in a production batch
  - Design for yield, design for manufacturability

- **Reliability**: ability of a circuit to conform to its specifications over a specified period of time and under specified conditions
  - Design for reliability: Methodologies to manage failure mechanisms in circuit design & layout

- **Robustness**:
  - Design for robustness
Objective

- Propose the reliability as a project criterion
- Propose an AMS/RF design for reliability methodology
  - Study the ageing physical phenomena
  - Propose and validate a model for reliability analysis and synthesis
Design Case

- RF front-end architecture for WLAN/WiMAX applications
- CMOS 65 nm
Physical Phenomena

- **HCl**: charges with sufficient kinetic energy to overcome a potential barrier

- **NBTI**: interface traps generated when under negative gate bias stress and at elevated temperature

- **TDDB**: gate oxide breakdown

- **EM**: erosions of the metal connections
Physical Phenomena (2)

- **HCl**: $V_{GD} \geq 0$ and $V_{GS} \gg 0$
  - Moderate Inversion ($V_{OV} \approx 200$ mV)

- **NBTI**: $V_{GS} \ll 0$ and temperature
  - Increase the recovery time and reduce the stress time

- **TDDB**: careful layout and leakage current control
  - Insufficient post-event models

- **EM**: careful layout and current density control
  - Reduce the number of passive components
Design for Reliability

Nominal Reliability Analysis

- Blocks’ $\Phi$
  - frequency, bandwidth, power consumption, noise, linearity, and gain

- $\Phi_{aged} = \Phi_{fresh} - \Delta\Phi$

- Block failure

- $\Delta\Phi$ impact for architecture performance
Nominal Reliability Analysis (2)

- Describe the application environment: test bench
- Evaluate the performances
  - Fresh vs. Aged
- Apply the model
- Find sensitive transistors

\[ I_{DSaged} = (1 - \alpha) I_{DSfresh} \]
Design Case for Model Validation

- Realistic DCO
- $f_{\text{osc}} = 1 \text{ GHz}$
- CMOS 65 nm
Model Validation

\[ e = \frac{f_{OSC\text{aged}} - f_{OSC\text{model}}}{f_{OSC\text{aged}}} \]

- Simulated in different stress times, temperatures and control voltages: \( \mu = 0.003 \) and \( \sigma = 0.037 \)

![Histogram of model error](image)
E.g. DCO at:

- $T = 27^\circ C$
- 10 years of ageing
Top-down Design Approach

RF front-end architecture for WLAN/WiMAX applications (CMOS 65 nm)
RF front-end Design for Reliability

- BLIXER
- DCO
- PGA

Architecture Specifications

**BLIXER:**
- $G = 14 \text{ dB}$
- $BW = 100 \text{ MHz}$ (single pole filter model),
- $NF = 3.5 \text{ dB}$
- $IP3 = 1.1 \text{ dBm}$

**DCO:**
- $P_{lo} = -2 \text{ dBm}$
- $L(1 \text{ MHz}) = -120 \text{ dBc/Hz at } f_{lo} = 5 \text{ GHz}$

**PGA:**
- $G = 20 \text{ dB}$
- $BW = 25 \text{ MHz}$ (single pole filter model),
- $NF = 30 \text{ dB}$
- $IP3 = -10 \text{ dBm}$

**TABLE I**

<table>
<thead>
<tr>
<th>Operational Frequency Bandwidth</th>
<th>1 GHz - 6 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>$&gt; 20 \text{ MHz}$</td>
</tr>
<tr>
<td>NF</td>
<td>$&gt; 30 \text{ dB}$</td>
</tr>
<tr>
<td>IP3</td>
<td>3.5 dB @ 1 GHz - 6 dB @ 6 GHz</td>
</tr>
<tr>
<td>S11</td>
<td>$&lt; 0 \text{ dBm}$</td>
</tr>
<tr>
<td></td>
<td>$&lt; -10 \text{ dB}$</td>
</tr>
</tbody>
</table>
Block Failure Model

**BLIXER:**
- $\Delta G = -3 \text{ dB}$,
- $\Delta NF = 1 \text{ dB}$,
- $\Delta IP3 = 1 \text{ dBm}$, and
- $\Delta BW = 50 \text{ MHz}$

**DCO:**
- $\Delta Plo = -3 \text{ dBm}$,
- $\Delta L(1\text{MHz}) = 10 \text{ dBC/Hz}$, and
- $\Delta flo = 0$ (by a ideal PLL)

**PGA:**
- $\Delta G = -3 \text{ dB}$,
- $\Delta NF = 10 \text{ dB}$,
- $\Delta IP3 = 1 \text{ dBm}$, and
- $\Delta BW = 10 \text{ MHz}$

**TABLE II**

<table>
<thead>
<tr>
<th>Test Case</th>
<th>PGA failure</th>
<th>DCO failure</th>
<th>BLIXER failure</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>no</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>1</td>
<td>no</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>2</td>
<td>no</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td>3</td>
<td>no</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>4</td>
<td>yes</td>
<td>no</td>
<td>no</td>
</tr>
<tr>
<td>5</td>
<td>yes</td>
<td>no</td>
<td>yes</td>
</tr>
<tr>
<td>6</td>
<td>yes</td>
<td>yes</td>
<td>no</td>
</tr>
<tr>
<td>7</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
</tbody>
</table>
Analytical Analysis

- $P = P_{BLIXER} + P_{DCO} + P_{PGA}$
- $\Delta P = \Delta P_{BLIXER} + \Delta P_{DCO} + \Delta P_{PGA}$
- $G = G_{BLIXER} + A_{LO} + G_{PGA}$
- $A_{LO} = \frac{V_{LO}}{V_{LO}'}$
- $\lim_{f \to BW} F = F_{BLIXER} + \frac{F_{PGA}}{G_{BLIXER}A_{LO}}$
- $IP3 = \frac{1}{\sqrt{IP3_{BLIXER}^2 + \frac{G^2_{BLIXER}A_{LO}^2}{IP3_{PGA}^2}}}$
Gain Reliability Result
NF Reliability Result
IP3 Reliability Result
Bottom-up Design Approach

Realistic DCO design for $f_{\text{osc}} = 1$ GHz at CMOS 65 nm
**DCO Design for Reliability**

**Design Eq.:**

\[ f_{osc} = \frac{1}{2N_{eff}t_d} \]

\[ t_d = \frac{C_L}{g_m} \]

\[ g_m = \frac{I_{DS}}{V_{ov}} \]

\[ f_{osc} = \frac{I_{DS}}{2N_{eff}C_LV_{ov}} \]

\[ P_{max} = N_{max}I_{BIAS}V_{DD} \]
Minimizing $V_{DD} - V_{BIAS}$, we decrease the power consumption and the NBTI degradation.
Phase Noise and Reliability

- Increase the size: better phase noise and worse reliability
- Increase phase noise: better reliability and area consumption

<table>
<thead>
<tr>
<th>W (μm)</th>
<th>Δf_{osc} @10 years</th>
<th>L(1.0 MHz) @1 GHz (dBc/Hz)</th>
<th>f_c (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>1.6%</td>
<td>-94.3</td>
<td>10.3</td>
</tr>
<tr>
<td>4</td>
<td>1.5%</td>
<td>-93.4</td>
<td>11.4</td>
</tr>
<tr>
<td>3</td>
<td>1.4%</td>
<td>-92.3</td>
<td>13.2</td>
</tr>
</tbody>
</table>

TABLE I

Phase Noise at 1 MHz off-set and its cut-off frequency (f_c) versus the oscillation frequency degradation (Δf_{osc}) at 10 years lifetime for each design sizing.
DCO Results

- **Area consumption:**
  - PMOS 9.0 μm/0.5 μm et NMOS 3.0 μm/0.5 μm

- **Oscillation Frequency:**
  - From 600 MHz to 1.2 GHz for $0.5 \text{ V} < V_{BIAS} < 0.6 \text{ V}$

- **Power consumption:** 850 μW before and 832 μW after 10 years of stress

- **Phase Noise:** -92.3 dBc/Hz for 1 MHz off-set and $f_c = 13.1 \text{ kHz}$
Variability Analysis

- 1000 points of Monte Carlo simulation: 10 years of stress
- Ageing can be neglected if compared to variability
Conclusions

- Reliability as a project criterion

- Reliability Synthesis: proposed and validated
  - Top-down – Explore the method in architectural level
  - Bottom-up – Explore the method in transistor level
Conclusions (2)

- **Reliability analysis:**
  - sensitive devices
  - how to increase the reliability

- **Physical phenomena:**
  - Impact
  - How to avoid
Challenges and Perspectives

- Variability-Aware Reliability vs Nominal Reliability Analysis
- Link Top-down and Bottom-up approaches
- Propose a common methodology to increase RF architectures reliability in advanced technologies (CMOS 65nm, CMOS 40nm)
  - Risk: Ageing models
Contributions

- Propose and validate the AMS/RF design for reliability methodology
- Propose and validate the reliability analysis tool in earlier design stages
- Manage the physical phenomena for quality purposes
Questions?

Thanks for your attention